

"EXPEDITED PROCEDURE"

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FACSIMILE

DATE:	March 31, 2003	REF. NO.:	09/583,617
ATTN:	Examiner Souw	FROM:	Robert J. Crawford
FAX NO.:	703-872-9319	DOCKET NO.	AMDA.441PA (TT3751)
PHONE NO.:		SUBJECT:	FINAL OFFICE ACTION RESPONSE with Amendment
NO. OF PAGES (w/ cover sheet):	11		

Includes authorization to charge Deposit Account 01-0365 (TT3751) new claims fees given on page 9 of this Response.

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Goruganthu	Examiner:	Souw, B.
Serial No.:	09/583,617	Group Art Unit:	2881
Filed:	May 31, 2000	Docket No.:	AMDA.441PA
Title:	ELECTRICAL PROBING OF SOI CIRCUITS		

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence and the papers, as described hereinabove, are being transmitted via facsimile only-Formal Entry, to the attention of Examiner Souw, Assistant Commissioner for Patents, Washington, D.C. 20231, on March 31, 2003.

Facsimile No. (703) 872-9319

By:

Kelly S. Walthers

FINAL OFFICE ACTION RESPONSE

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BOX AF
Assistant Commissioner for Patents
Washington, D.C. 20231

MAR 31 2003

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Dear Sir:

In response to the Office Action mailed on January 29, 2003, please amend the Application as follows and consider the following remarks. Payment for the new claims is provided herein in the remarks below.

In the Specification:

04/04/2003 TDW/KMS 00000000 010365 09583617

01 FC:1202

90.00 CH

Please replace the indicated paragraphs as follows:

On page 6, beginning on line 7:

FIG. 1 shows a portion of a flip chip die 100 exemplifying one type of a variety of dies having SOI structure to which the present invention is applicable. The die of FIG. 1 is shown in an inverted position with the back side facing up, such as would be a flip die bonded to a package substrate. A very thin buried oxide (BOX) 150 is formed over silicon substrate 160, and a thin layer of silicon 140 is formed on the oxide 150. Source/drain regions 120 and 130 are formed in the thin layer of silicon 140. A gate 110,